FIG. 1A

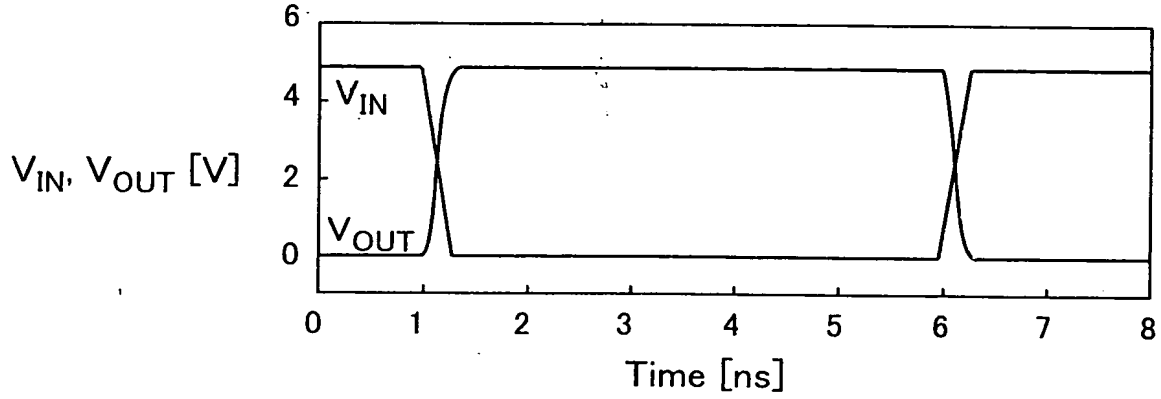


FIG. 1B

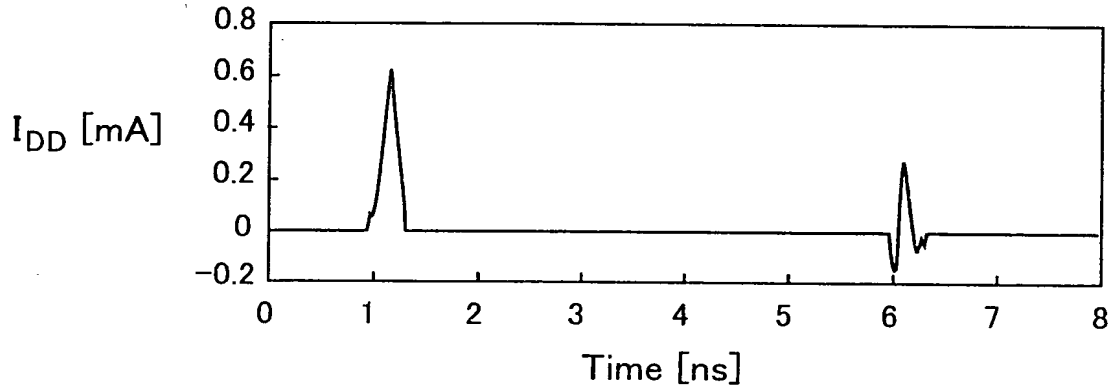


FIG. 1C

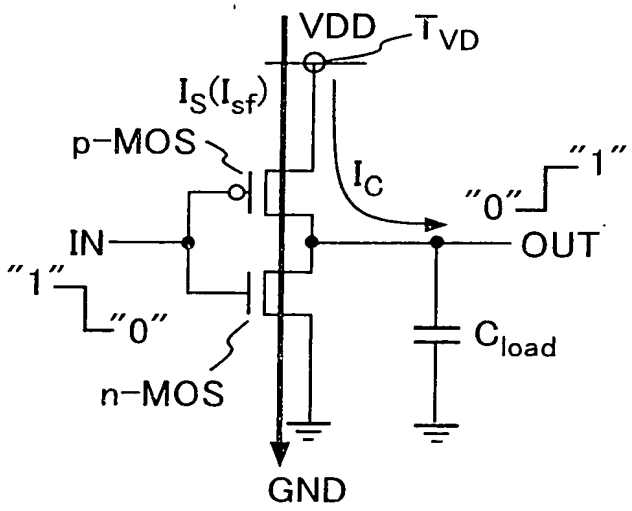


FIG. 1D

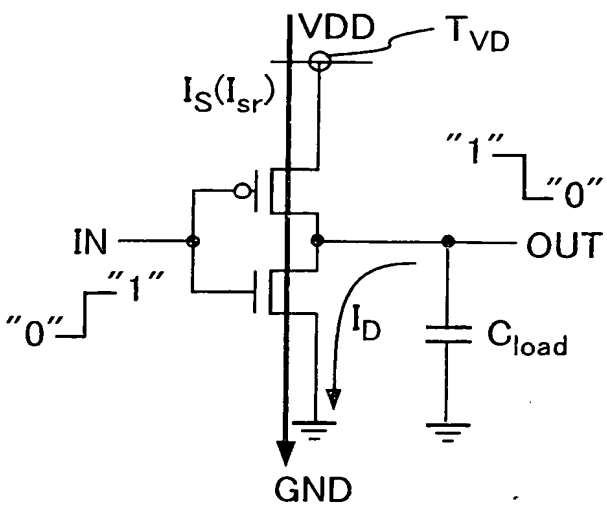


FIG. 2 A

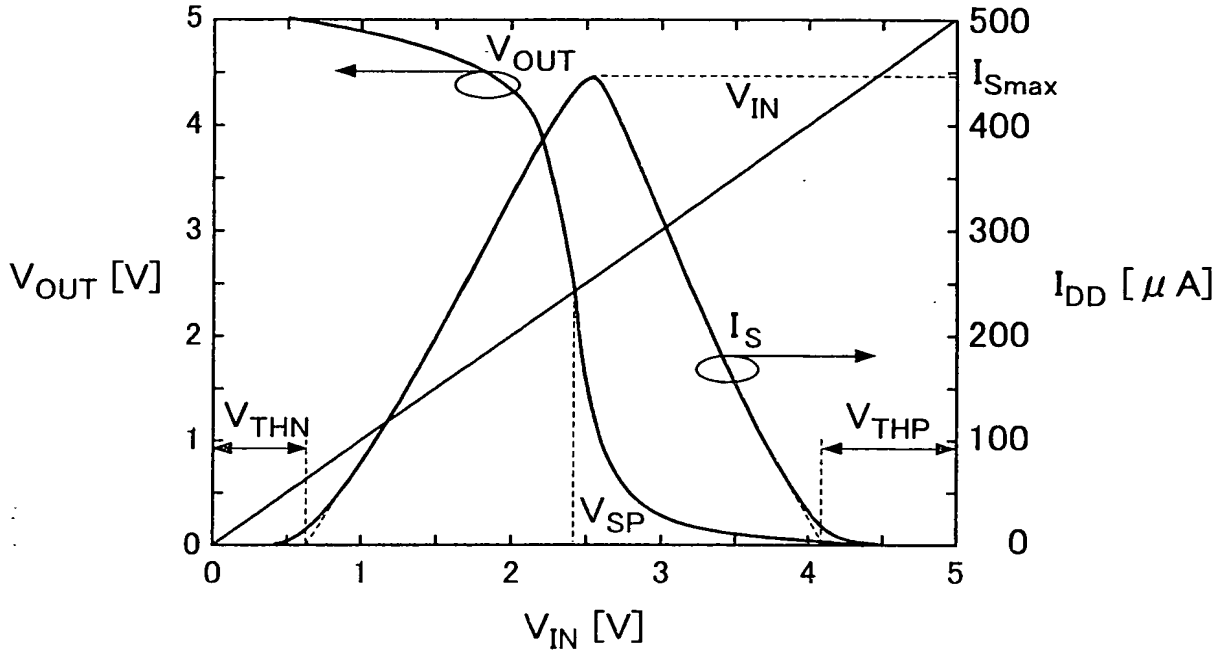

5
4
3
2
1
0
500
400
300
200
100
0
V_{OUT}
I_{Smax}
V_{IN}
I_S
V_{THN}
V_{THP}
V_{SP}
V_{OUT} [V]
I_{DD} [μA]
0
1
2
3
4
5
V_{IN} [V]

FIG. 2 B

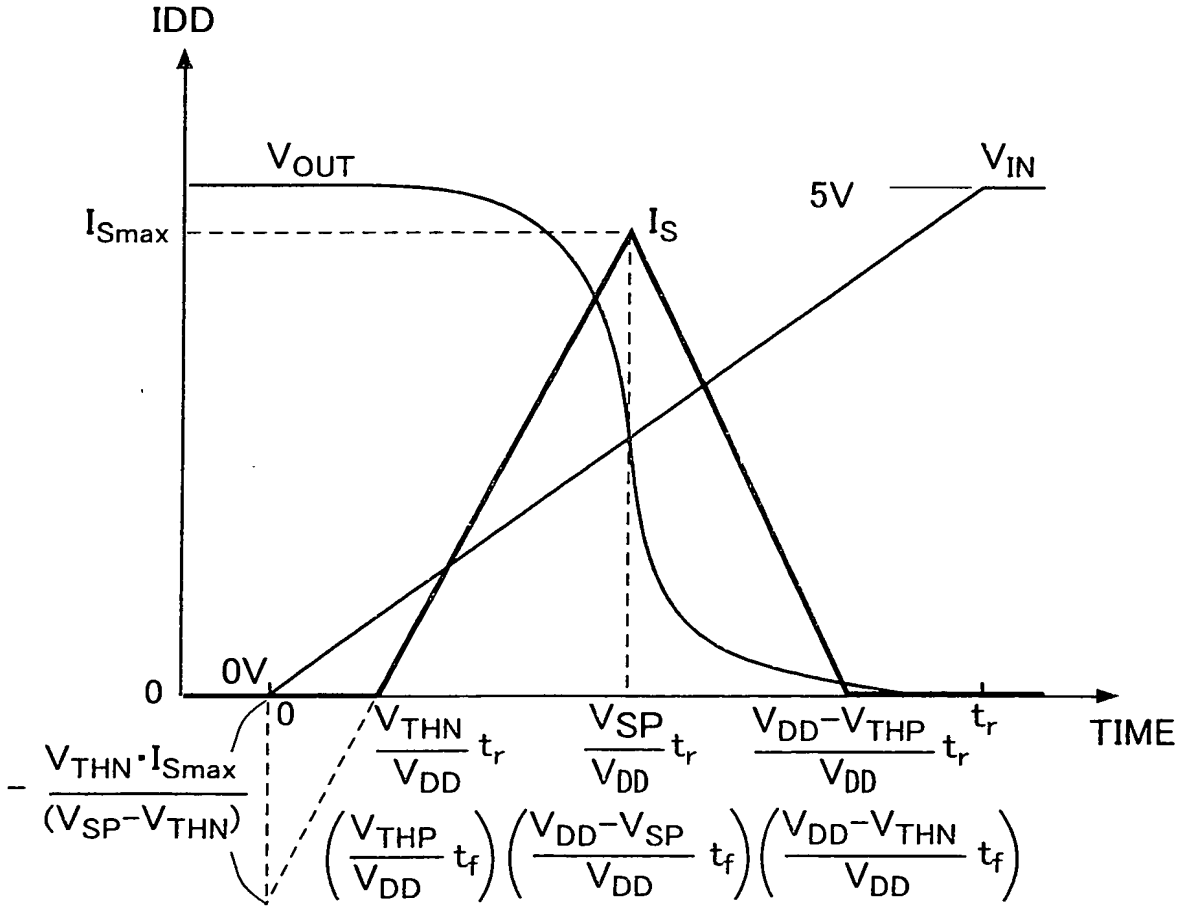

IDD
V_{OUT}
V_{IN}
5V
I_{Smax}
I_S
0V
0
TIME
$-\frac{V_{THN} \cdot I_{Smax}}{(V_{SP}-V_{THN})}$
$\frac{V_{THN}}{V_{DD}} t_r$
$\frac{V_{SP}}{V_{DD}} t_r$
$\frac{V_{DD}-V_{THP}}{V_{DD}} t_r$
t_r
$\left(\frac{V_{THP}}{V_{DD}} t_f\right)$
$\left(\frac{V_{DD}-V_{SP}}{V_{DD}} t_f\right)$
$\left(\frac{V_{DD}-V_{THN}}{V_{DD}} t_f\right)$

FIG. 3 A

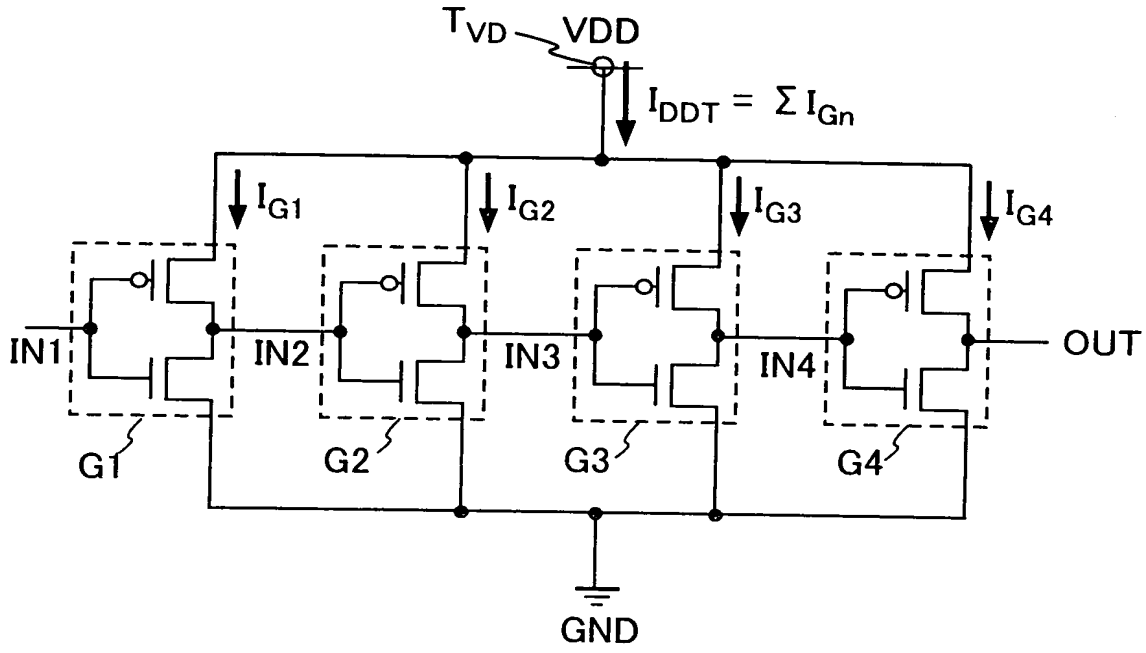


FIG. 3 B

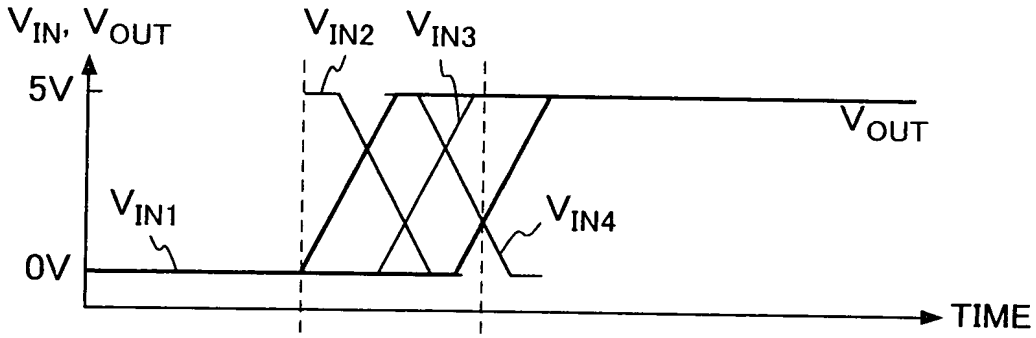


FIG. 3 C

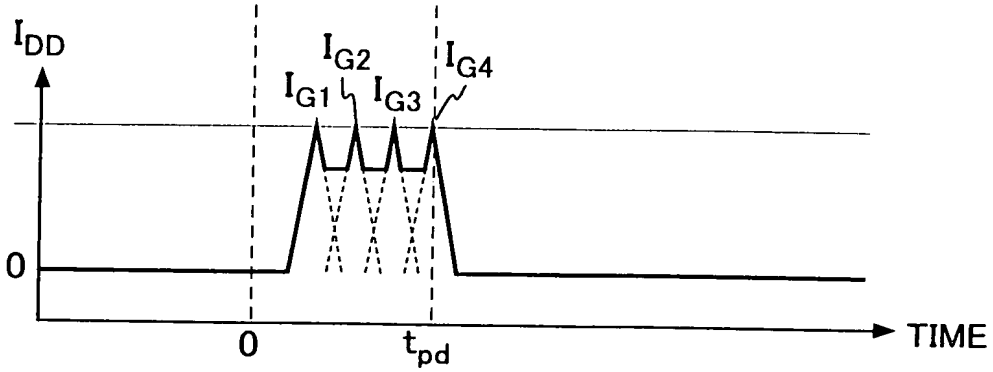


FIG. 4 A

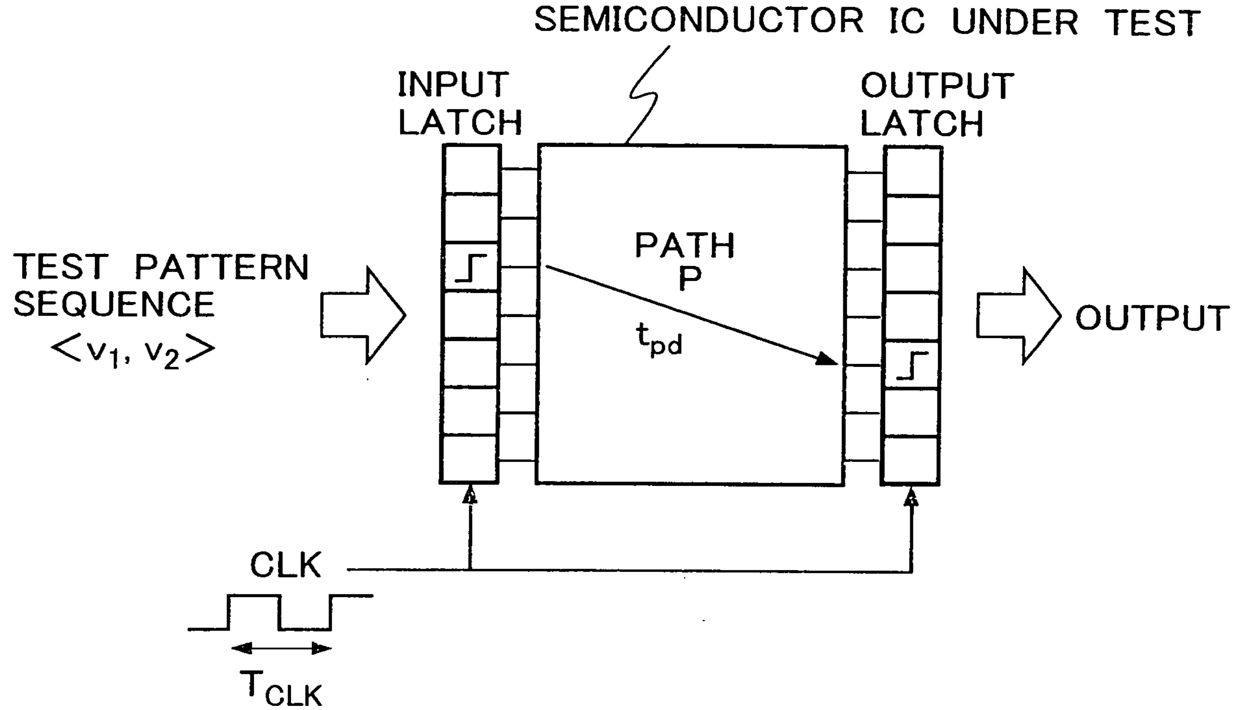


FIG. 4 B

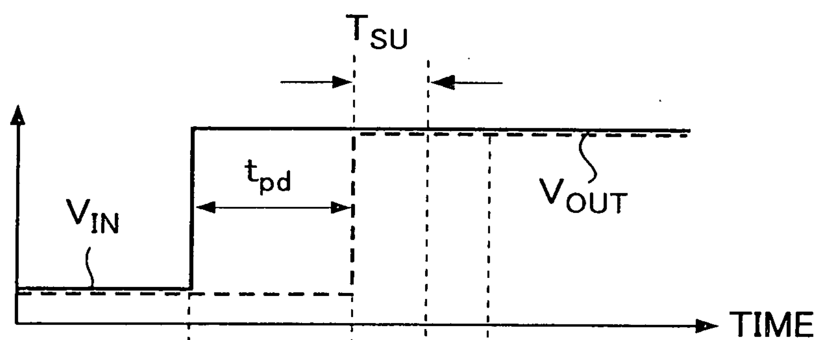


FIG. 4 C

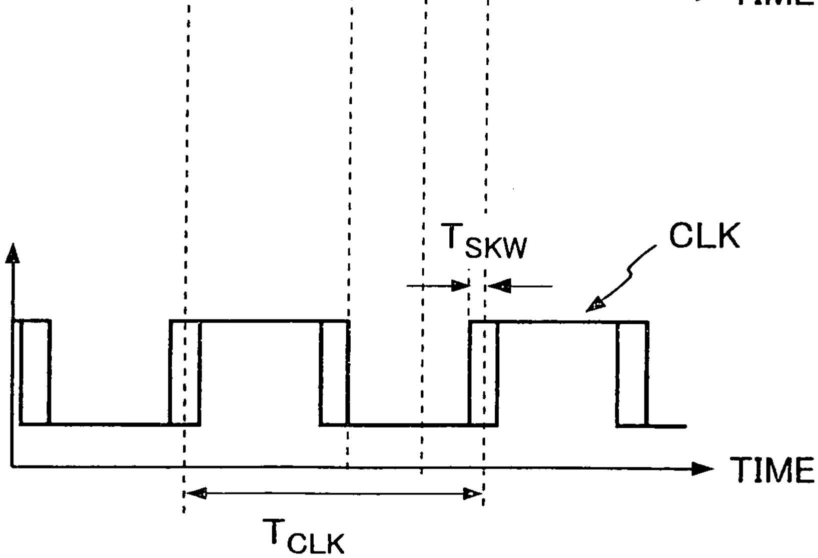


FIG. 5 A

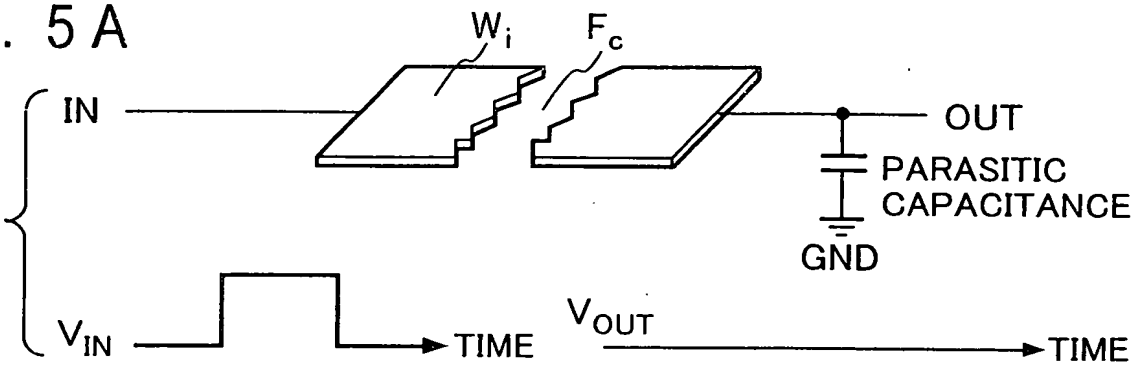


FIG. 5 B

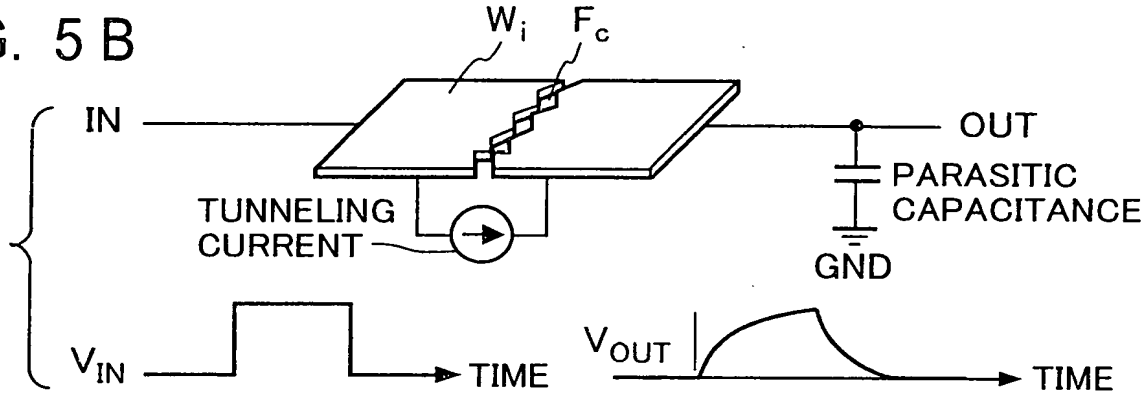


FIG. 6 A

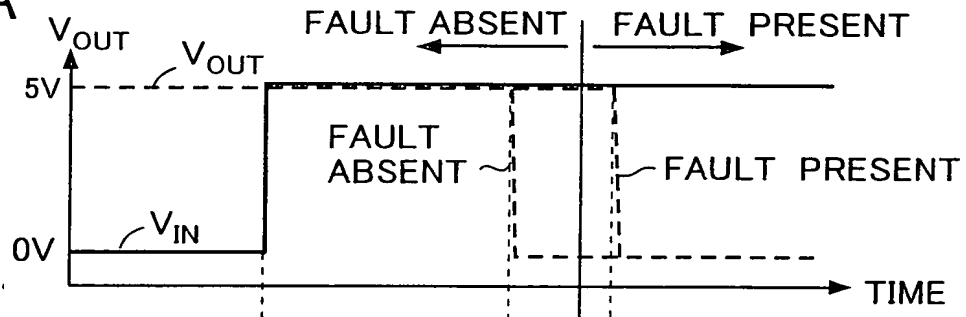


FIG. 6 B

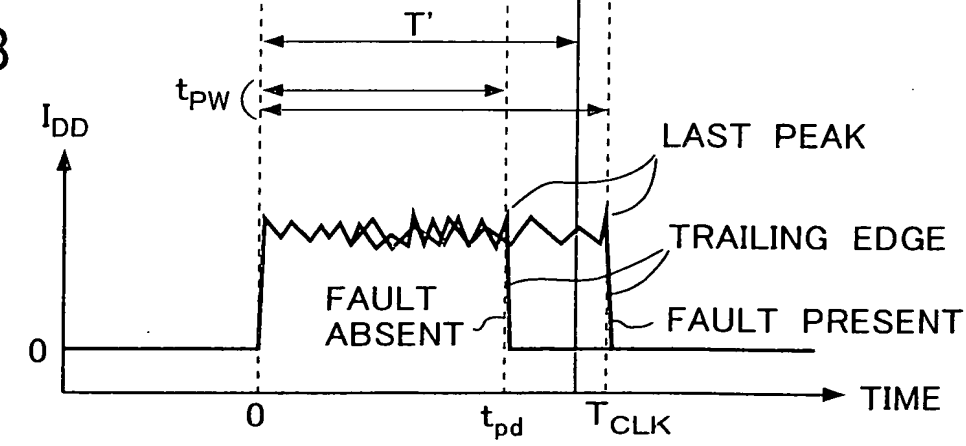


FIG. 7 A

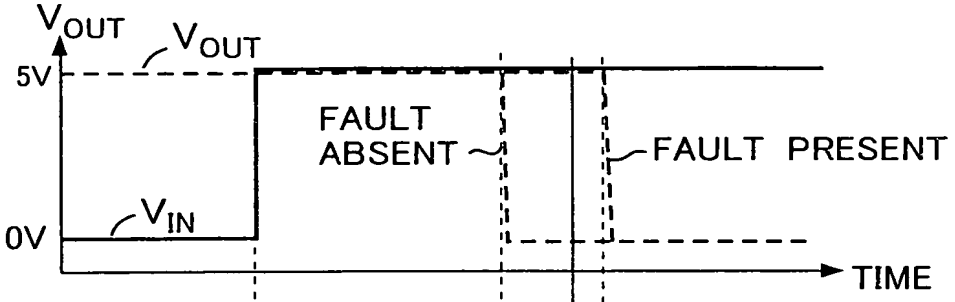
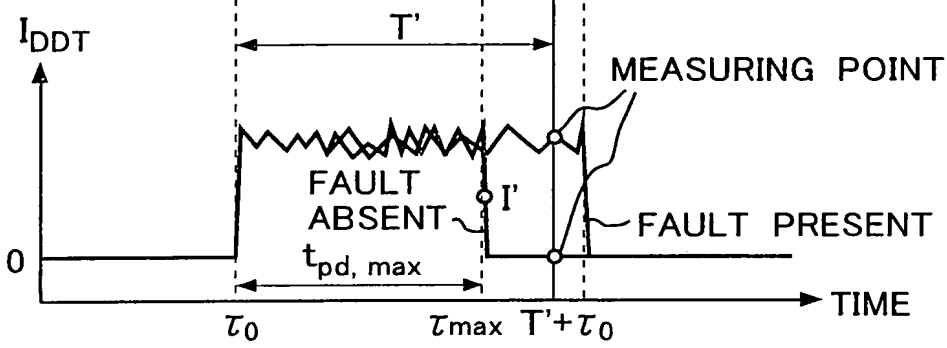


FIG. 7 B



FAULT ABSENT : $i_{DDT}(T'+\tau_0) \leq I'$

FAULT PRESENT : $i_{DDT}(T'+\tau_0) > I'$

FIG. 8

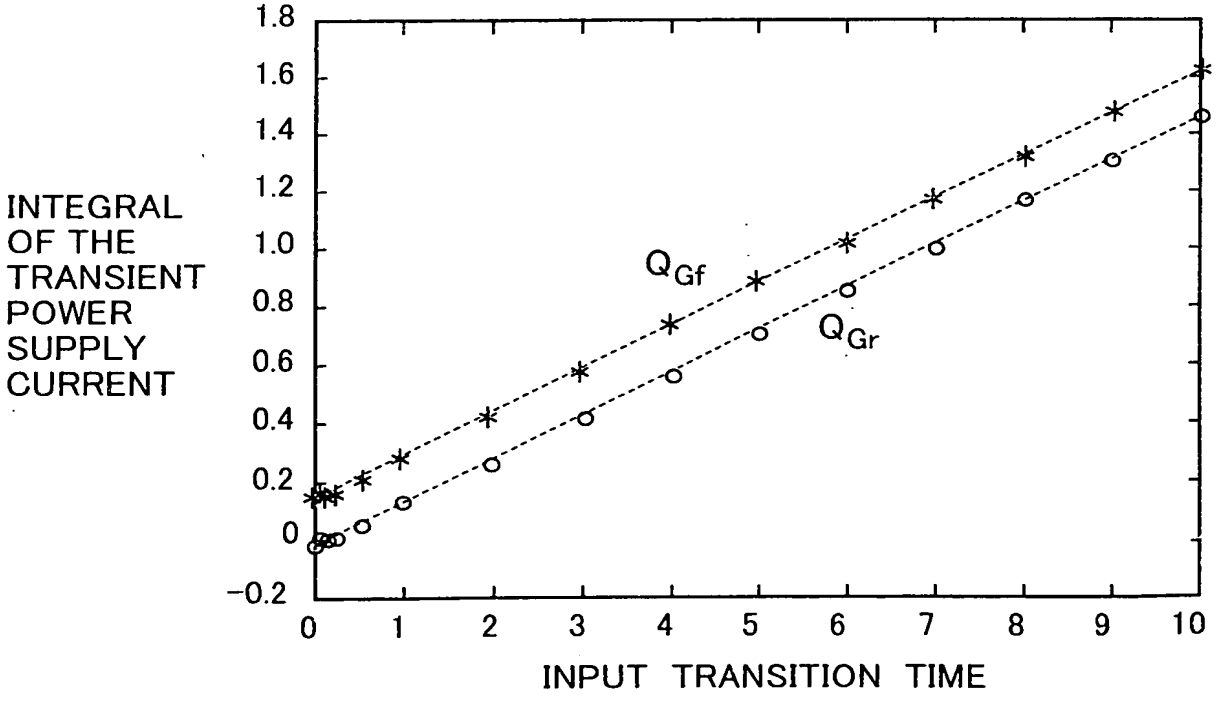


FIG. 9 A

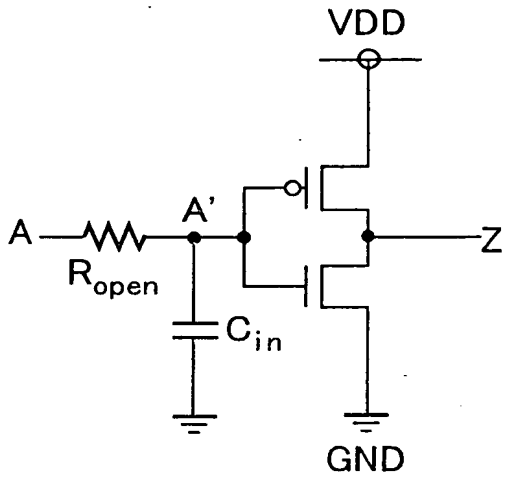


FIG. 9 B

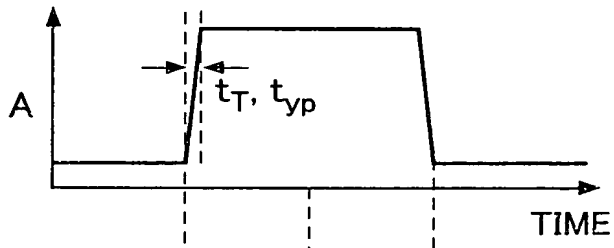


FIG. 9 C

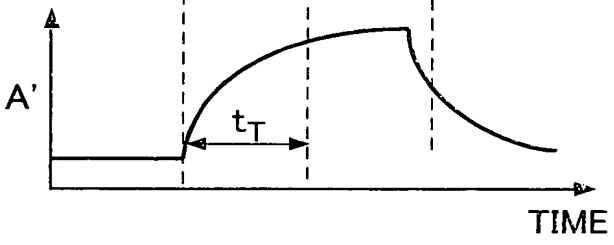


FIG. 10

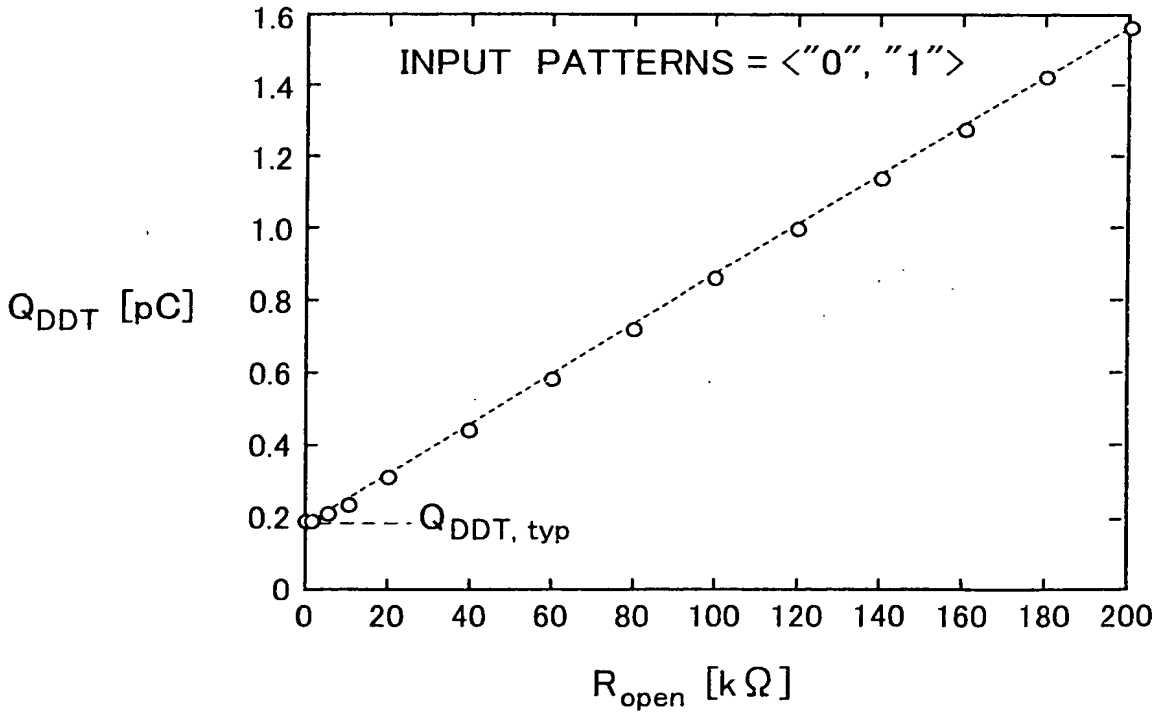


FIG. 11

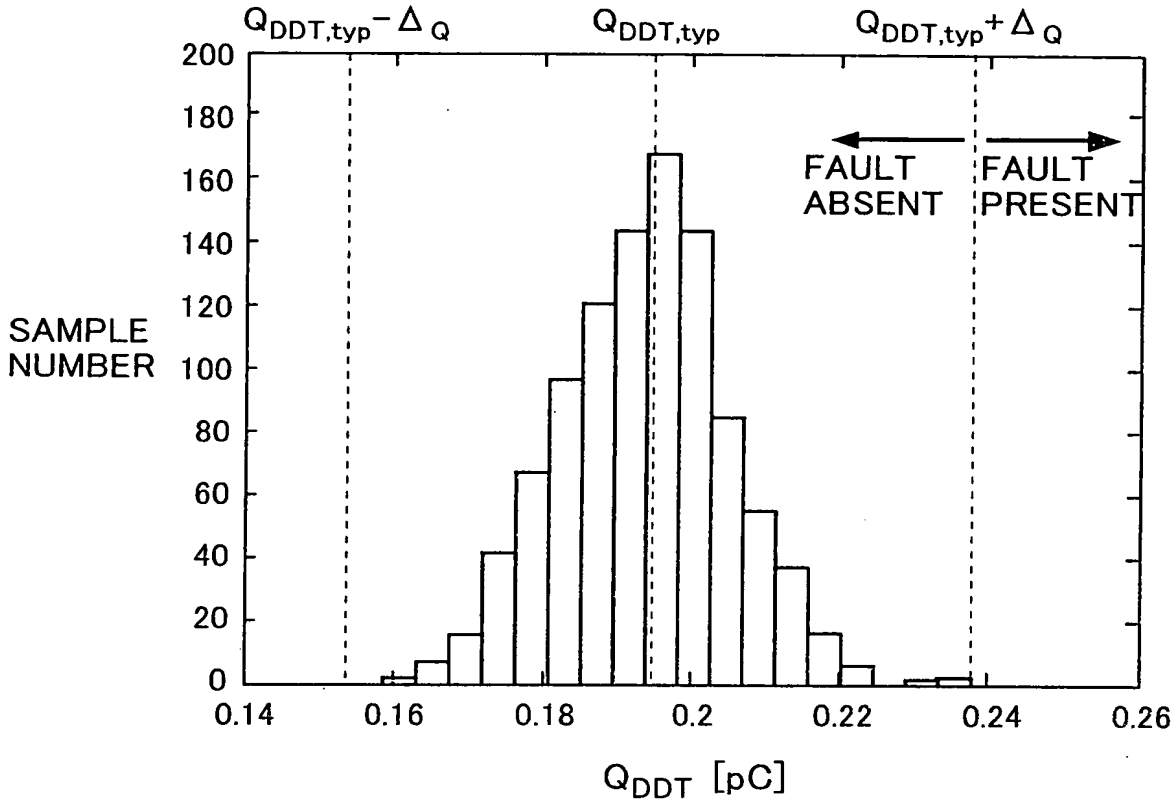

$Q_{DDT,typ}-\Delta_Q$
$Q_{DDT,typ}$
$Q_{DDT,typ}+\Delta_Q$
FAULT ABSENT
FAULT PRESENT
SAMPLE NUMBER
200
180
160
140
120
100
80
60
40
20
0
0.14
0.16
0.18
0.2
0.22
0.24
0.26
Q_{DDT} [pC]

FIG. 12

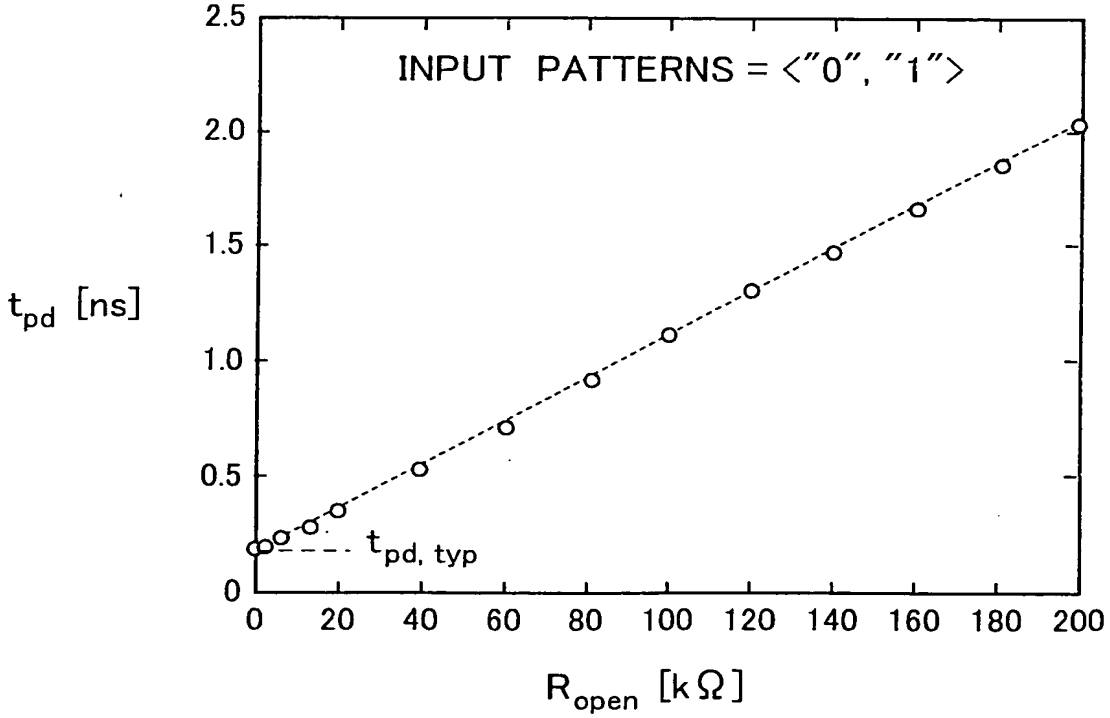

INPUT PATTERNS = <"0", "1">
t_{pd} [ns]
2.5
2.0
1.5
1.0
0.5
0
$t_{pd, typ}$
0
20
40
60
80
100
120
140
160
180
200
R_{open} [kΩ]

FIG. 13

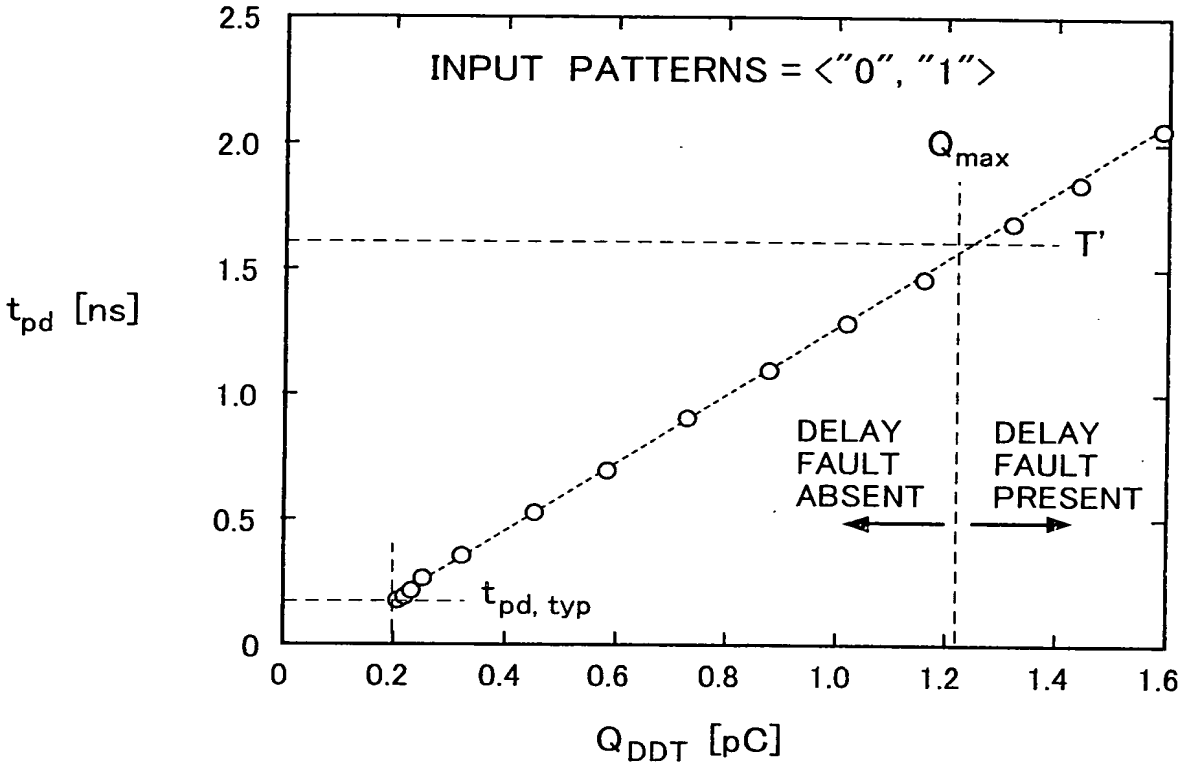

INPUT PATTERNS = <"0", "1">
Q_{max}
T'
t_{pd} [ns]
DELAY FAULT ABSENT
DELAY FAULT PRESENT
$t_{pd, typ}$
2.5
2.0
1.5
1.0
0.5
0
0 0.2 0.4 0.6 0.8 1.0 1.2 1.4 1.6
Q_{DDT} [pC]

FIG. 14

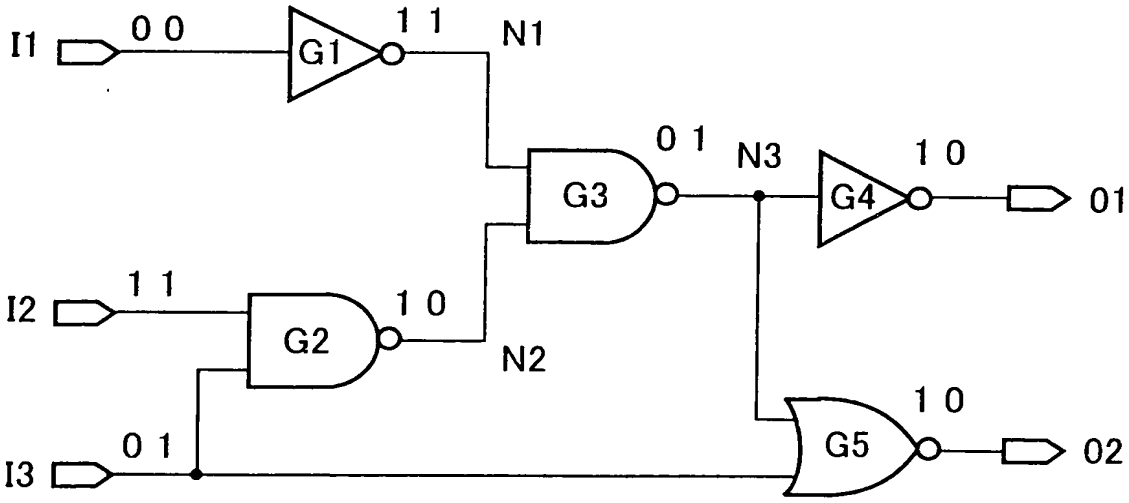

I1
0 0
G1
1 1
N1
0 1
N3
G3
1 0
G4
01
I2
1 1
G2
1 0
N2
I3
0 1
1 0
G5
02

FIG. 15

TEST PATTERN SEQUENCE IDENTIFIER	INPUT TERMINAL			INTERNAL NODE			OUTPUT TERMINAL		FAULT-DETECTABLE GATE
	I1	I2	I3	N1	N2	N3	O1	O2	
T1	0	0	R	1	1	0	1	F	G5
T2	0	1	R	1	F	R	F	F	G2, G3, G4, G5
T3	1	0	R	0	1	1	0	0	–
T4	1	1	R	0	F	1	0	0	G2
T5	0	R	0	1	1	0	1	1	–
T6	0	R	1	1	F	R	F	0	G2, G3, G4
T7	1	R	0	0	1	1	0	0	–
T8	1	R	1	0	F	1	0	0	G2
T9	R	0	0	F	1	R	F	F	G1, G3, G4, G5
T10	R	0	1	F	1	R	F	0	G1, G3, G4
T11	R	1	0	F	1	R	F	F	G1, G3, G4, G5
T12	R	1	1	F	0	1	0	0	G1
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮

FIG. 16

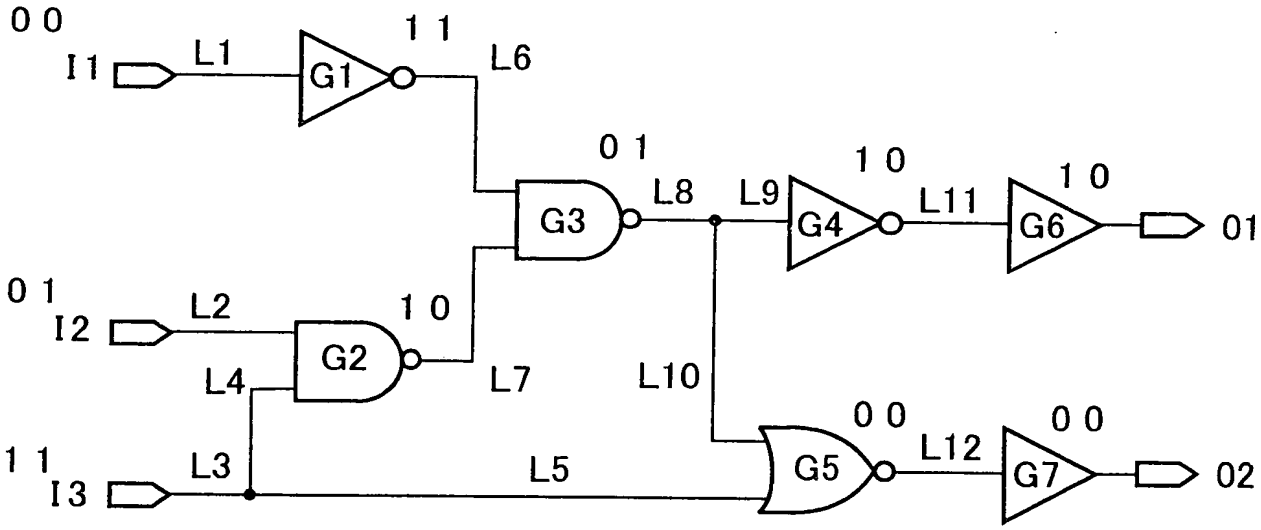

0 0
I1
L1
G1
1 1
L6
0 1
G3
L8
L9
1 0
G4
L11
1 0
G6
01
0 1
I2
L2
G2
1 0
L7
L4
L10
1 1
I3
L3
L5
0 0
G5
L12
0 0
G7
02

FIG. 17

TEST PATTERN SEQUENCE IDENTIFIER	INPUT TERMINAL			INTERNAL SIGNAL LINE												OUTPUT TERMINAL		FAULT-DETECTABLE INTERNAL SIGNAL LINE
	I1	I2	I3	1	2	3	4	5	6	7	8	9	10	11	12	01	02	
T1	0	0	R	0	0	R	R	R	1	1	1	1	1	1	F	1	F	L3, L5, L12
T2	0	1	R	0	1	R	R	R	1	F	F	F	F	F	F	F	F	L3, L4, L5, L7, L8, L9, L10, L11, L12
T3	1	0	R	1	0	R	R	R	0	1	0	0	0	0	0	0	0	–
T4	1	1	R	1	1	R	R	R	0	F	0	0	0	0	0	0	0	L3, L4
T5	0	R	0	0	R	0	0	0	1	1	1	1	1	1	1	1	1	–
T6	0	R	1	0	R	1	1	1	1	F	F	F	F	F	0	F	0	L2, L7, L8, L9, L11
T7	1	R	0	1	R	0	0	0	0	1	0	0	0	0	0	0	0	–
T8	1	R	1	1	R	1	1	1	0	F	0	0	0	0	0	0	0	L2
T9	R	0	0	R	0	0	0	0	F	1	F	F	F	F	F	F	F	L1, L6, L8, L9, L10, L11, L12
T10	R	0	1	R	0	1	1	1	F	1	F	F	F	F	0	F	0	L1, L6, L8, L9, L11
T11	R	1	0	R	1	0	0	0	F	1	F	F	F	F	F	F	F	L1, L6, L8, L9 L10, L11, L12
T12	R	1	1	R	1	1	1	1	F	0	0	0	0	0	0	0	0	L1
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮

FIG. 18

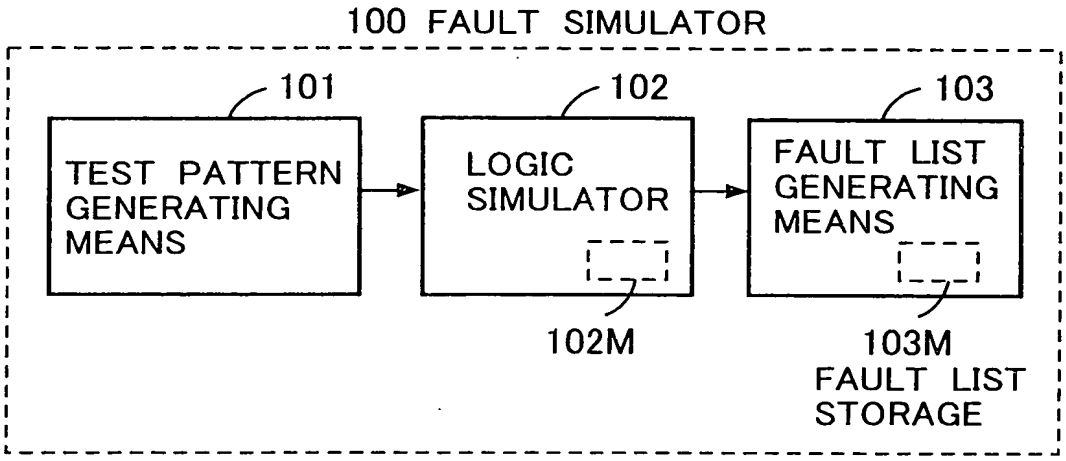

100 FAULT SIMULATOR
101
TEST PATTERN GENERATING MEANS
102
LOGIC SIMULATOR
102M
103
FAULT LIST GENERATING MEANS
103M
FAULT LIST STORAGE

FIG. 19

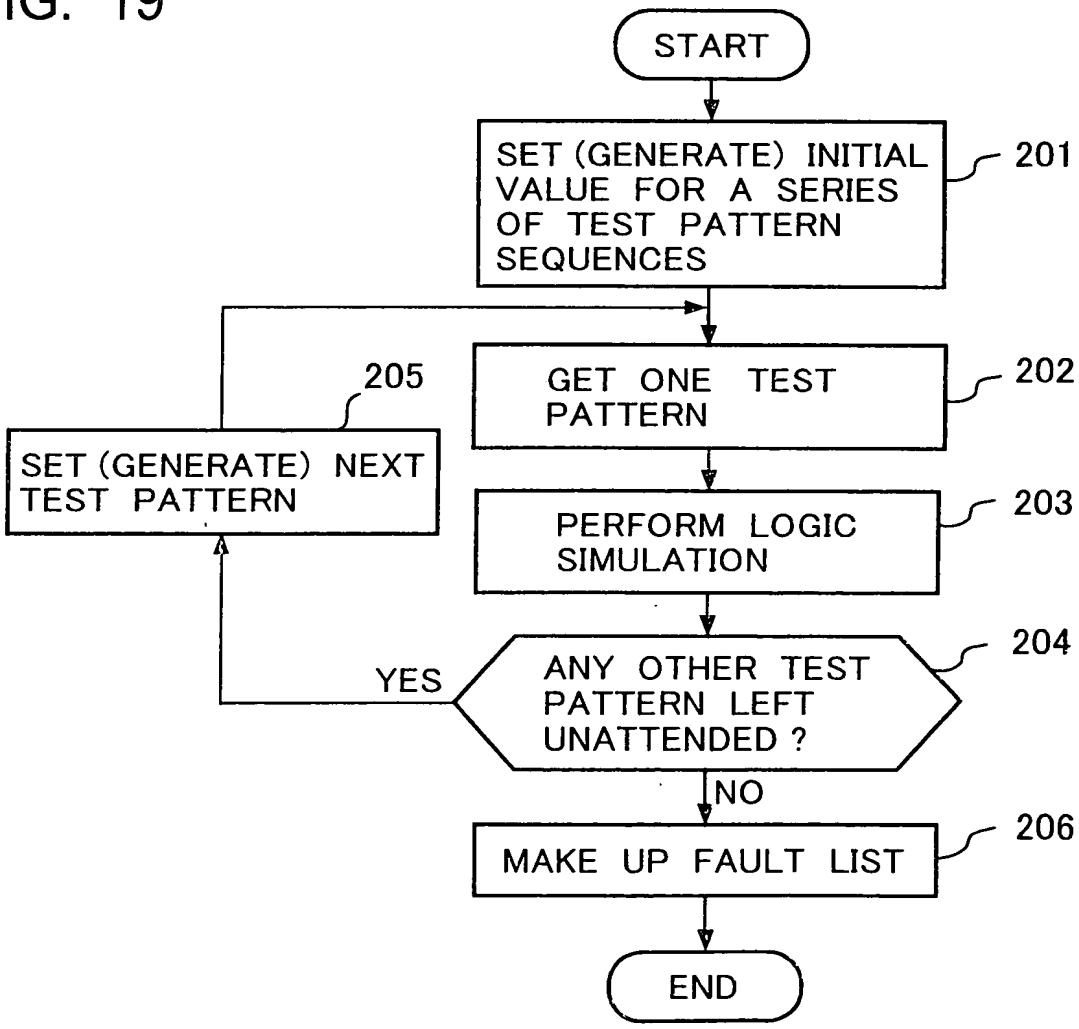

START
SET (GENERATE) INITIAL VALUE FOR A SERIES OF TEST PATTERN SEQUENCES
201
GET ONE TEST PATTERN
202
PERFORM LOGIC SIMULATION
203
ANY OTHER TEST PATTERN LEFT UNATTENDED ?
204
YES
NO
SET (GENERATE) NEXT TEST PATTERN
205
MAKE UP FAULT LIST
206
END

FIG. 20

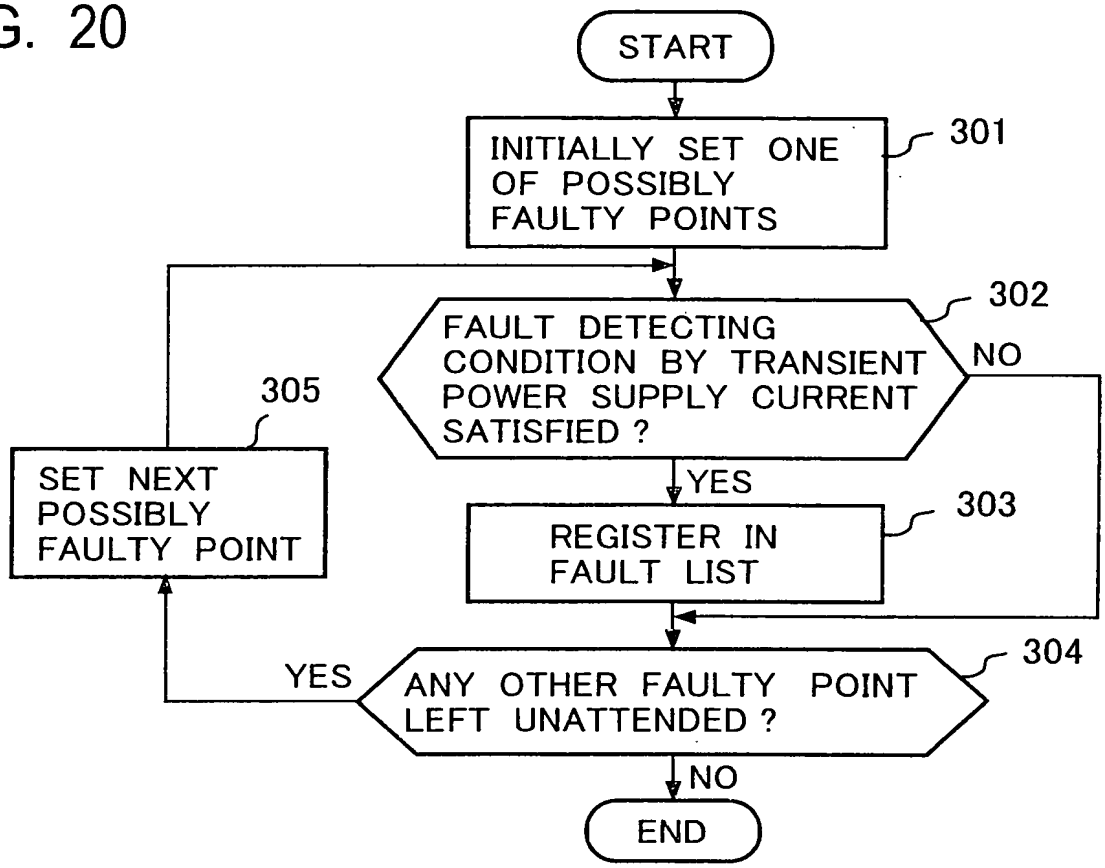


FIG. 21

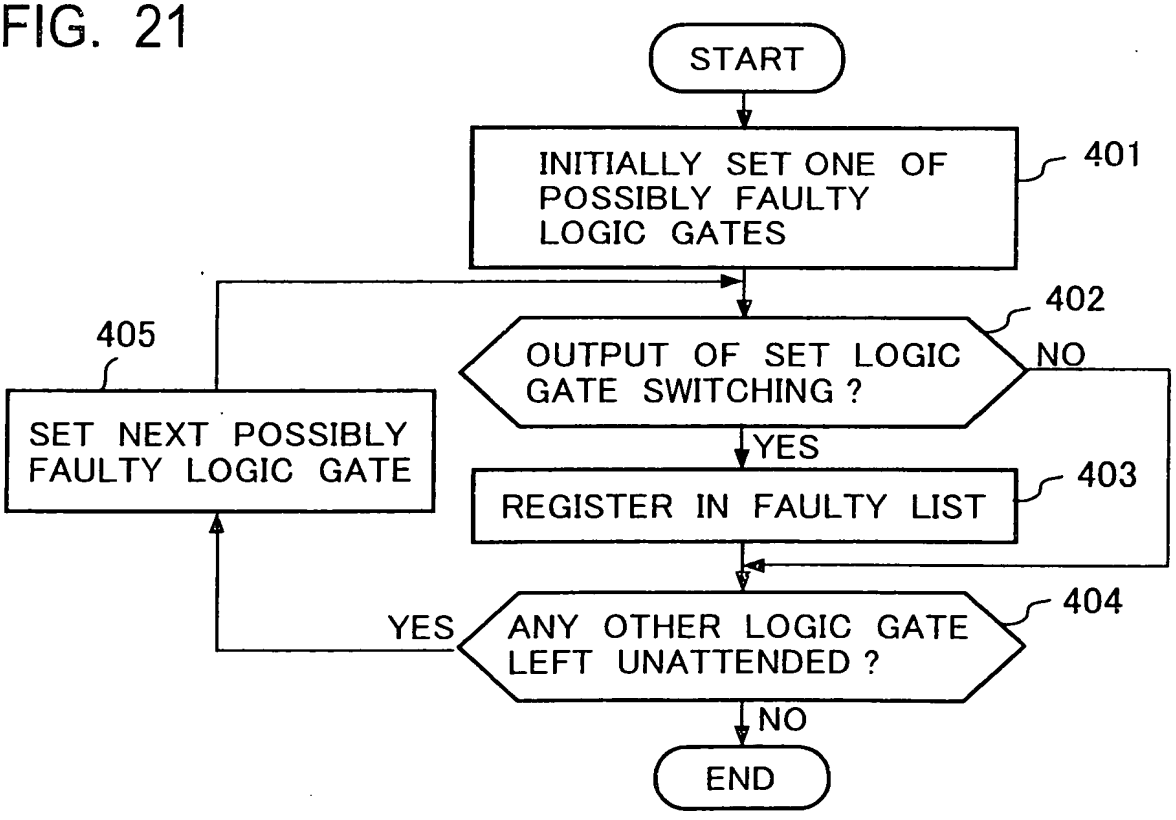


FIG. 22

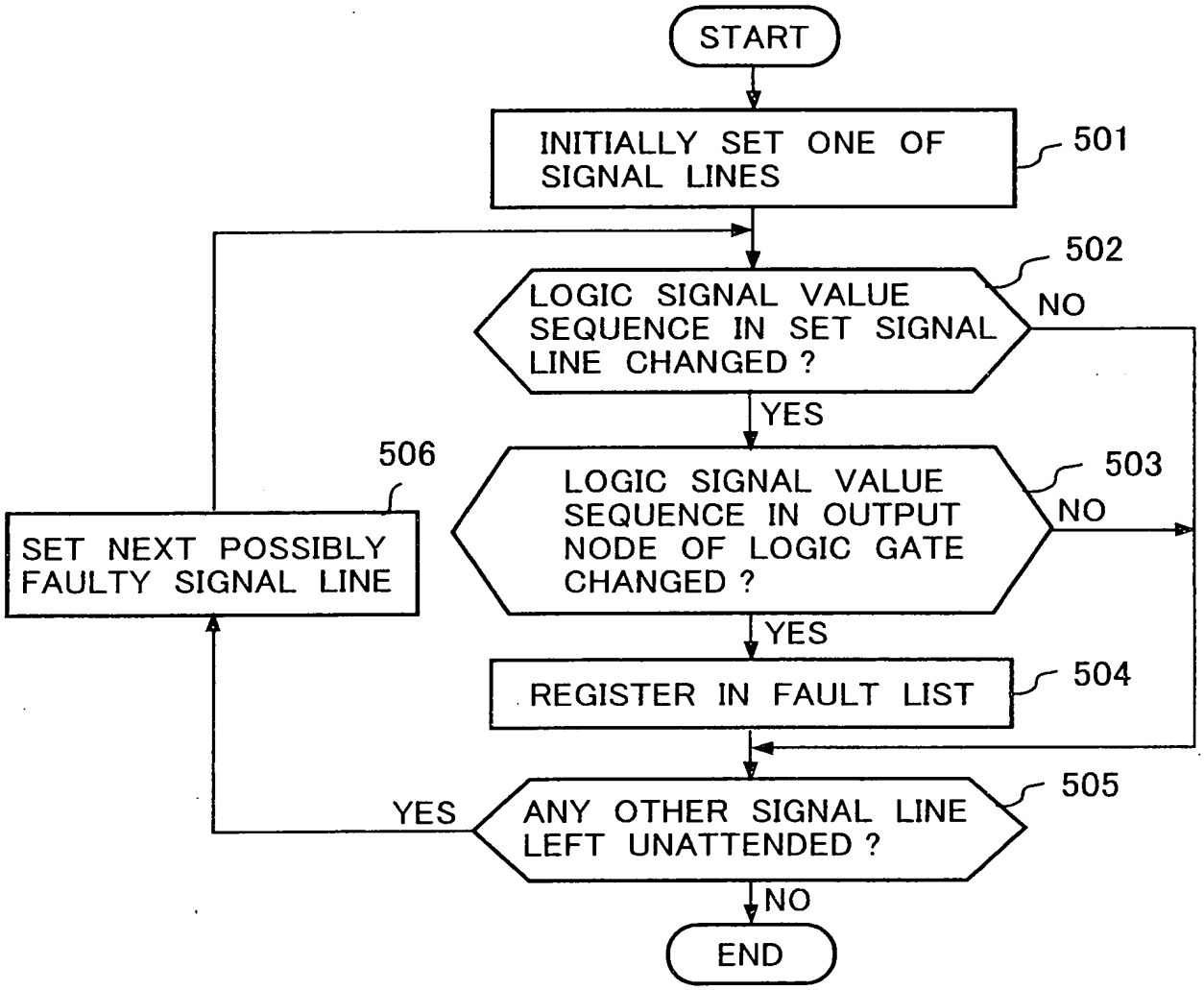

START
INITIALLY SET ONE OF SIGNAL LINES
501
LOGIC SIGNAL VALUE SEQUENCE IN SET SIGNAL LINE CHANGED ?
502
NO
YES
LOGIC SIGNAL VALUE SEQUENCE IN OUTPUT NODE OF LOGIC GATE CHANGED ?
503
NO
YES
REGISTER IN FAULT LIST
504
ANY OTHER SIGNAL LINE LEFT UNATTENDED ?
505
YES
NO
SET NEXT POSSIBLY FAULTY SIGNAL LINE
506
END

FIG. 23

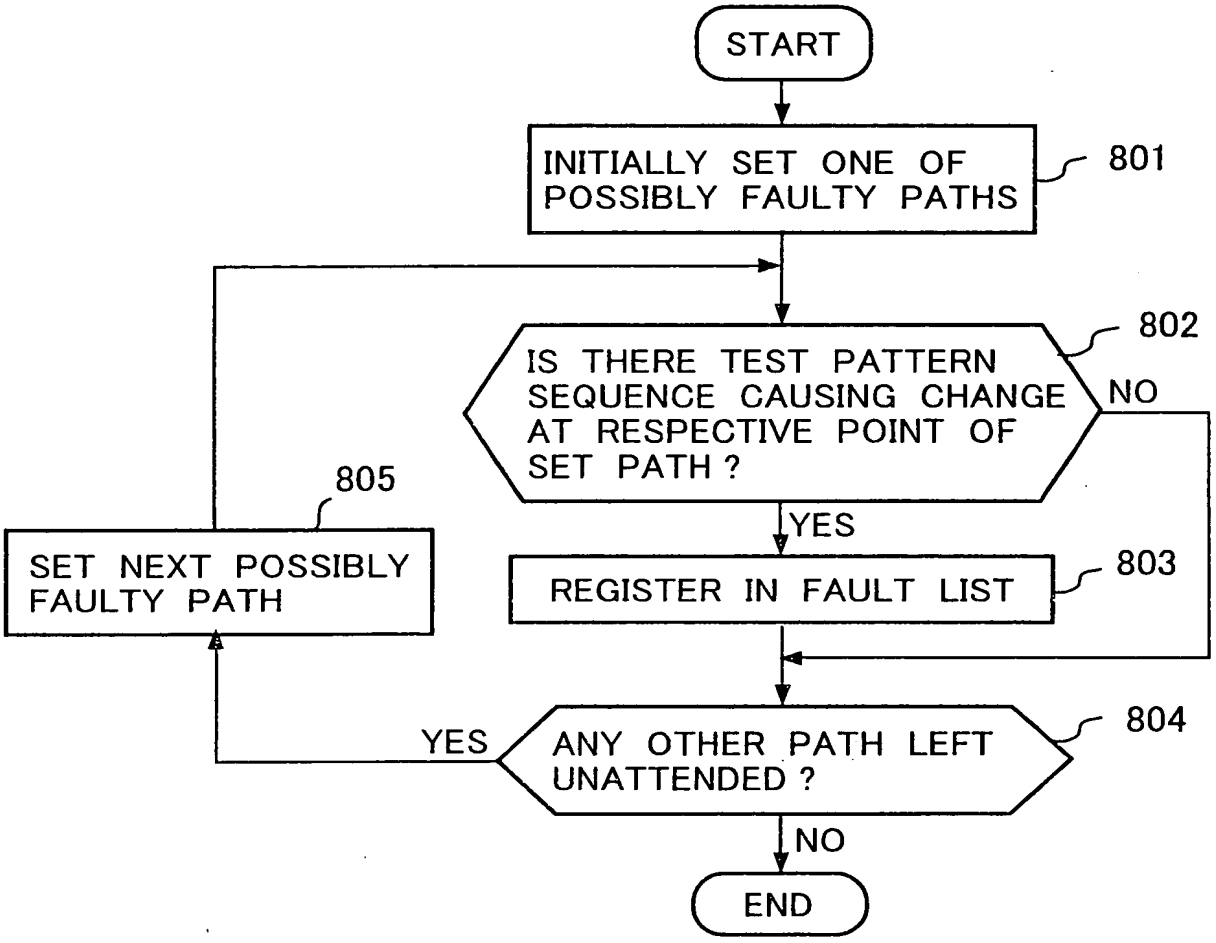

START
INITIALLY SET ONE OF POSSIBLY FAULTY PATHS
801
IS THERE TEST PATTERN SEQUENCE CAUSING CHANGE AT RESPECTIVE POINT OF SET PATH ?
802
NO
YES
REGISTER IN FAULT LIST
803
ANY OTHER PATH LEFT UNATTENDED ?
804
YES
NO
SET NEXT POSSIBLY FAULTY PATH
805
END

FIG. 24

TEST PATTERN SEQUENCE IDENTIFIER	INPUT TERMINAL			INTERNAL NODE			OUTPUT TERMINAL		FAULT-DETECTABLE PATH
	I1	I2	I3	N1	N2	N3	O1	O2	
T1	0	0	R	1	1	0	1	F	<I3, O2>
T2	0	1	R	1	F	R	F	F	<I3, N2, N3, O1>, <I3, N2, N3, O2>
T3	1	0	R	0	1	1	0	0	-
T4	0	1	R	0	F	1	0	0	-
T5	0	R	0	1	1	0	1	1	-
T6	0	R	1	1	F	R	F	0	<I2, N2, N3, O1>
T7	1	R	0	0	1	1	0	0	-
T8	1	R	1	0	F	1	0	0	-
T9	R	0	0	F	1	R	F	F	<I1, N1, N3, O1>, <I1, N1, N3, O2>
T10	R	0	1	F	1	R	F	0	<I1, N1, N3, O1>
T11	R	1	0	F	1	R	F	F	<I1, N1, N3, O1>, <I1, N1, N3, O2>
T12	R	1	1	F	0	1	0	0	-
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮

FIG. 25

TEST PATTERN SEQUENCE IDENTIFIER	INPUT TERMINAL 1 2 3	INTERNAL SIGNAL LINE 1 2 3 4 5 6 7 8 9 10 11 12	OUTPUT TERMINAL 1 2	FAULT-DETECTABLE PATH
T1	0 0 R	0 0 R R R 1 1 1 1 1 1 F	1 F	<I3, L3, L5, L12, O2>
T2	0 1 R	0 1 R R R 1 F F F F F F	F F	<I3, L3, L5, L12, O2> <I3, L3, L4, L7, L8, L9, L11, O1> <I3, L3, L4, L7, L8, L10, L12, O1>
T3	1 0 R	1 0 R R R 0 1 0 0 0 0 0	0 0	–
T4	1 1 R	1 1 R R R 0 F 0 0 0 0 0	0 0	–
T5	0 R 0	0 R 0 0 0 1 1 1 1 1 1 1	1 1	–
T6	0 R 1	0 R 1 1 1 1 F F F F F 0	F 0	<I2, L2, L7, L8, L9, L11, O1>
T7	1 R 0	1 R 0 0 0 0 1 0 0 0 0 0	0 0	–
T8	1 R 1	1 R 1 1 1 0 F 0 0 0 0 0	0 0	–
T9	R 0 0	R 0 0 0 0 F 1 F F F F F	F F	<I1, L1, L6, L8, L9, L11, O1> <I1, L1, L6, L8, L10, L12, O2>
T10	R 0 1	R 0 1 1 1 F 1 F F F F 0	F 0	<I1. L1, L6, L8, L9, L11, O1>
T11	R 1 0	R 1 0 0 0 F 1 F F F F F	F F	<I1, L1, L6, L8, L9, L11, O1> <I1, L1, L6, L8, L10, L12, O2>
T12	R 1 1	R 1 1 1 1 F 0 0 0 0 0 0	0 0	–
⋮	⋮ ⋮ ⋮	⋮ ⋮ ⋮ ⋮ ⋮ ⋮ ⋮ ⋮ ⋮ ⋮ ⋮ ⋮	⋮ ⋮	⋮

FIG. 26

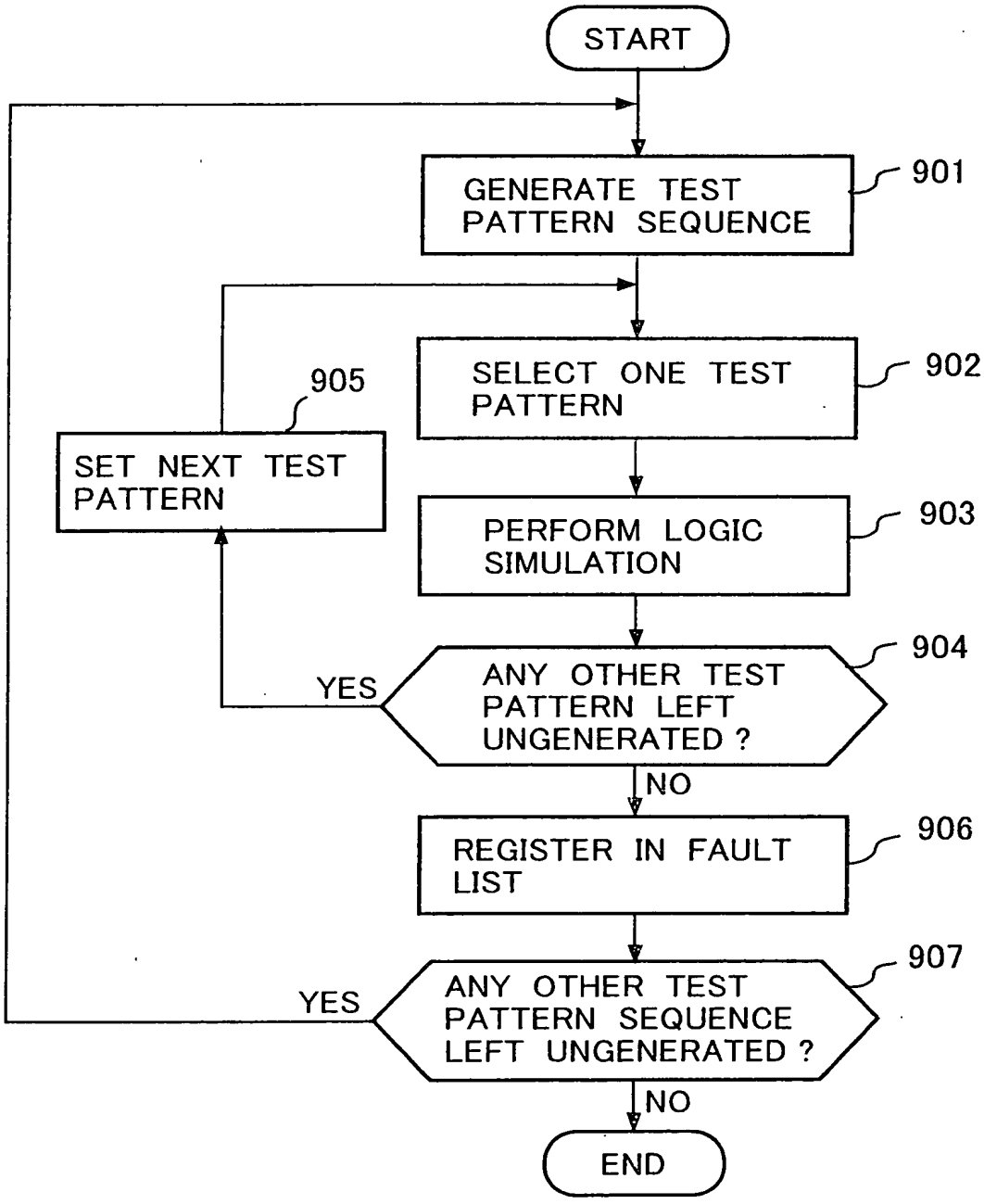

START
GENERATE TEST PATTERN SEQUENCE
901
SELECT ONE TEST PATTERN
902
PERFORM LOGIC SIMULATION
903
ANY OTHER TEST PATTERN LEFT UNGENERATED ?
904
YES
NO
SET NEXT TEST PATTERN
905
REGISTER IN FAULT LIST
906
ANY OTHER TEST PATTERN SEQUENCE LEFT UNGENERATED ?
907
YES
NO
END

FIG. 27

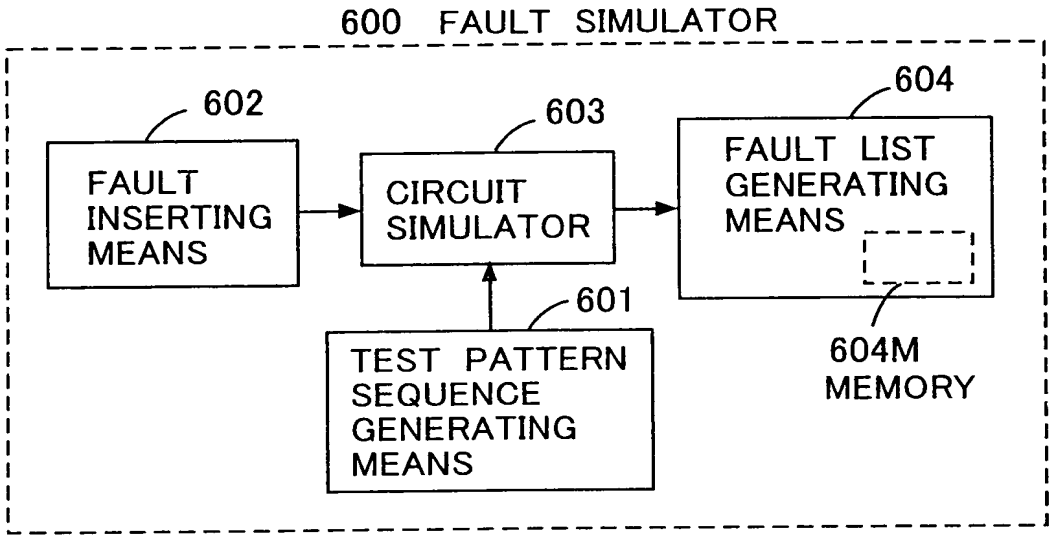
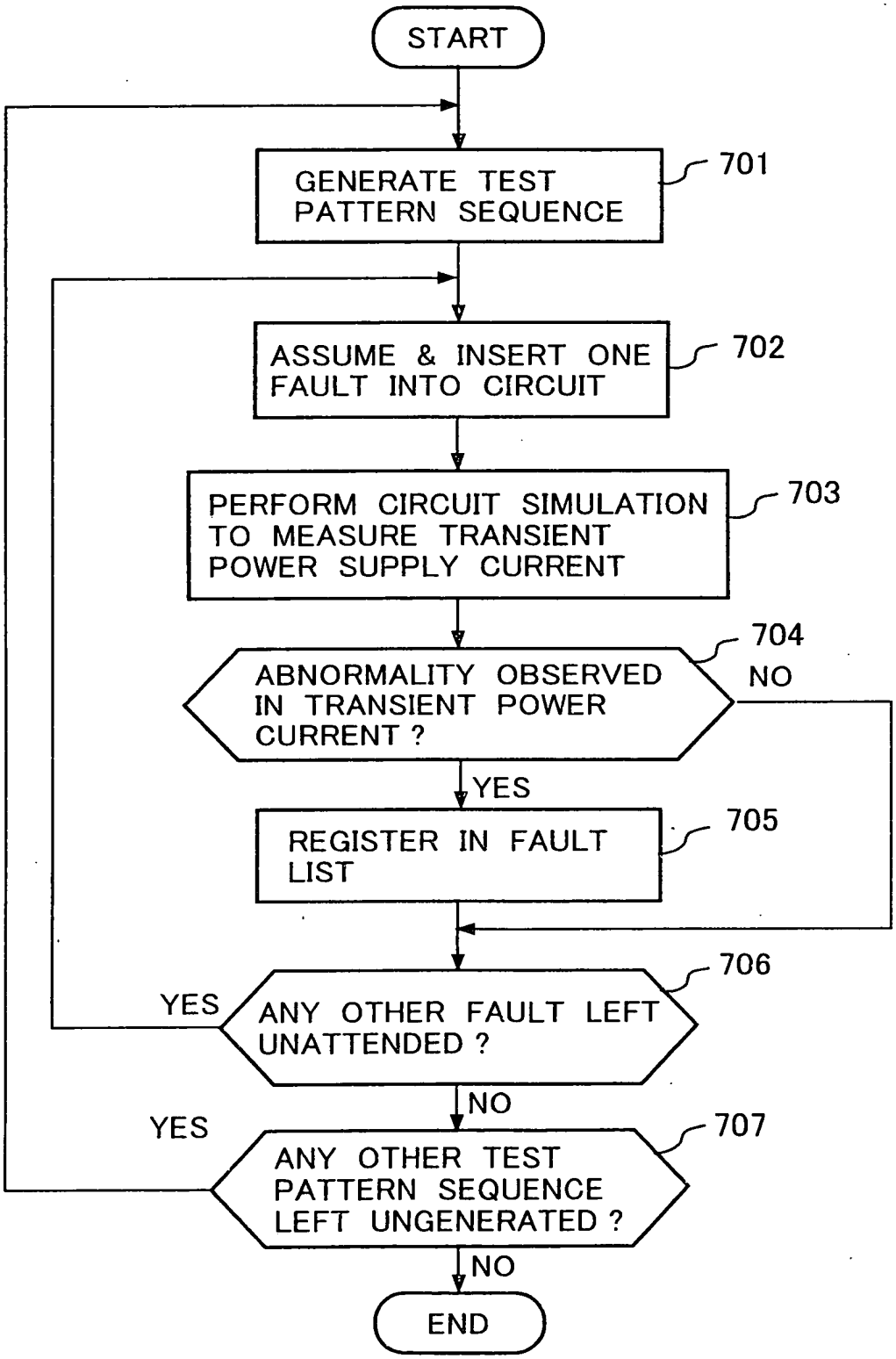

600 FAULT SIMULATOR
602
FAULT INSERTING MEANS
603
CIRCUIT SIMULATOR
604
FAULT LIST GENERATING MEANS
604M MEMORY
601
TEST PATTERN SEQUENCE GENERATING MEANS

FIG. 28


START
GENERATE TEST PATTERN SEQUENCE
701
ASSUME & INSERT ONE FAULT INTO CIRCUIT
702
PERFORM CIRCUIT SIMULATION TO MEASURE TRANSIENT POWER SUPPLY CURRENT
703
ABNORMALITY OBSERVED IN TRANSIENT POWER CURRENT ?
704
NO
YES
REGISTER IN FAULT LIST
705
ANY OTHER FAULT LEFT UNATTENDED ?
706
YES
NO
ANY OTHER TEST PATTERN SEQUENCE LEFT UNGENERATED ?
707
YES
NO
END